IN THE CLAIMS:

Amendment of the claims

Please amend claims 1, 3, 5, 8 and 11 as follows:

Listing of the claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) The image display device ~~being~~ is characterized in that a first signal line group, constituted of a plurality of first signal lines which are arranged in parallel, and a second signal line group, constituted of a plurality of second signal lines which are arranged in parallel in a region adjacent to the group of first signal lines, are formed on a substrate, and

a dummy line is arranged between the first signal line group and the second signal line group.

2. (original) The image display device according to claim 1, wherein both ends of the dummy line are not connected to other signal lines.

3. (currently amended) The image display device according to claim 1, wherein the dummy line has ~~each~~ one portion thereof connected to the first signal ~~lines~~ line or ~~the~~ a second signal line which is arranged adjacent to the dummy line.

4. (original) The image display device according to any one of claims 1 to 3, wherein the dummy line is constituted of a plurality of lines which are arranged in parallel.

5. (currently amended) The image display device ~~being~~ is characterized in that a drive circuit which supplies signals to respective pixels in an image display part of a substrate through signal lines is formed outside the image display part,

the drive circuit is constituted of a plurality of semiconductor devices, and the respective semiconductor devices are configured such that data ~~are~~ is supplied between these respective semiconductor devices and other semiconductor devices, which are arranged adjacent to these respective semiconductor devices, through data transfer signal lines, and

a dummy line is formed between the signal lines and the data transfer signal lines.

6. (original) The image display device according to claim 5, wherein the signal lines are drain signal lines which supply video signals to respective pixels, and the drive circuit constitutes a video signal drive circuit.

7. (original) The image display device according to claim 5, wherein the signal lines are gate signal lines which supply scanning signals to respective pixels, and the drive circuit constitutes a scanning signal drive circuit.

8. (currently amended) The image display device according to claim 5, wherein ~~the~~ signal lines which are arranged adjacent to each other are formed into ~~a~~ ~~group~~ groups,

the signal lines which are formed into each group are directed in ~~the~~ a converging direction outside the image display part and are connected to ~~the~~ respective semiconductor devices, and data transfer signal lines which connect

between ~~the~~ one semiconductor device and another semiconductor device that is arranged adjacent to the ~~former~~ one semiconductor device are formed such that the data transfer signal lines ~~wrap~~ loop around area at the image display part side ~~than~~ between these respective semiconductor devices.

9. (original) The image display device according to claim 5, wherein the dummy lines are connected with the signal lines which are arranged adjacent to the dummy lines.

10. (original) Image display device according to claim 9, wherein the connection between the dummy lines and the signal lines are established at the image display part side.

11. (currently amended) An image display device ~~being~~ is characterized in that a pair of electrodes are formed on each pixel within an image display part of a substrate, one of the pair of electrodes includes a counter electrode to which a counter voltage supply signal which becomes ~~the~~ a reference with respect to signals supplied to another electrode of the pair of electrodes is supplied,

a drive circuit which supplies signals to the respective pixels through signal lines is formed outside the pixel display part, the drive circuit is constituted of a plurality of semiconductor devices, a counter voltage supply signal line which supplies counter voltage supply signals to the counter electrode is formed on a region between ~~the~~ one semiconductor device and another semiconductor device which is arranged adjacent to the ~~former~~ one semiconductor device, and

a dummy line is arranged between the signal lines and the counter voltage supply signal line.